REMARKS

Claims 16-30 are pending in this application. By this Amendment, claims 16 and 17 are amended. No new matter is added. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

Applicants appreciate the courtesies shown to Applicants' representatives by Examiner Memula in the July 24, 2007 personal interview. Applicants' separate record of the substance of the interview is incorporated into the following remarks.

The Office Action objects to claim 16 for a number of formalities. Claim 16 has been amended to overcome the objections of the Office Action. Additionally, the Office Action rejects claims 16-30 under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 16 and 17 have been amended to more particularly point out and more distinctly claim the pending subject matter, in order to overcome this rejection. Claims 18-30 are allowable, at least due to their dependence on proper claims 16 and 17.

The Office Action rejects claims 16-30 under 35 U.S.C. §112, second paragraph. The Office Action also rejects claims 16-28 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,946,899 to Myono. Further, the Office Action rejects claim 29 under 35 U.S.C. §103 as being unpatentable over Myono in view of U.S. Patent Application Publication No. 2002/0014663 to Iwamatsu et al. (hereinafter "Iwamatsu"); and claim 30 under 35 U.S.C. §103(a) as being unpatentable over Myono in view of at least any of U.S. Patent Application Publications Nos. 2004/0077151 to Bhattacharyya, 2004/0087084 to Hsieh, 2004/0094763 to Agnello et al. (hereinafter "Agnello"), and 2004/0018668 to Maszara. The Applicant's respectfully traverse these rejections.

The Office Action asserts that Myono teaches an integrated circuit with two subassemblies. As illustrated by Fig. 1, these two subassemblies are driven by four clock signals. The first subassembly consists of transistors M3 and M4, and op-amps S3 and S4.

the second assembly consists of transistors M1 and M2, and inverting op-amps S1 and S2, according to the Office Action. However, Myono teaches that this configuration consists of four functional elements M1-M4, which are each independent stages of a circuit, as discussed in the abstract. Further, each subassembly is connected to an op-amp via its gate input. Each gate input is connected to the output of an op-amp in the case of an NPN transistor, or an inverting op-amp, in the case of a PNP transistor. These op-amps receive two different clock signals and output a third signal, resulting from the input clock signals.

As shown in Fig. 1, no two op-amps will output the same signal, because no two op-amps receive the same two input clock signals. Specifically, S1 receives CLK' and CLKB, S2 receives CLK and CLKB', S3 receives CLK and CLK' and S4 CLKB and CLKB'.

In contrast, the claimed invention teaches an integrated circuit "wherein a same clock signal is applied to the clock input of all subassemblies." Myono does not teach this feature, because Myono requires that multiple unique clock signals be synthesized for each transistor subassembly M1-M4 from four separate clock signals.

For at least the above reasons, Myono does not anticipate, nor does it render obvious, the subject matter of the pending claims. Further, claims 17-30 are allowable for at least their dependence on allowable independent claim 16, as well as for the separately patentable subject matter described therein.

Accordingly, reconsideration and withdrawal of the rejection of the subject matter of claims 16-30 as being anticipated under 35 U.S.C. §102(e) is respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 16-30 are earnestly solicited.

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Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

William P. Berridge Registration No. 30,024

Kirk D. Berkhimer Registration No. 59,874

WPB:ARK/hms

Date: July 27, 2007

OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320

Telephone: (703) 836-6400

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